CLAIMS

1. A multiple-state memory cell, comprising:

a first electrode layer formed from a first conductive material;

a second electrode layer formed from a second conductive material;

a first layer of a metal-doped chalcogenide material disposed between the first and second electrode layers, the first layer providing a medium in which a conductive growth can be formed to electrically couple together the first and second electrode layers;

a third electrode layer formed from a third conductive material; and

a second layer of a metal-doped chalcogenide material disposed between the second and third electrode layers, the second layer providing a medium in which a conductive growth can be formed to electrically couple together the second and third electrode layers.

2. The memory cell of claim 1 wherein the first conductive material comprises a composition of a silver material.

3. The memory cell of claim 1 wherein at least one of the first or second layers of metal-doped chalcogenide material is a material selected from the group consisting of germanium selenide, arsenic sulfide, germanium telluride, and germanium sulfide.

4. The memory cell of claim 1 wherein the material of at least one of the first or second layers of metal-doped chalcogenide material comprises a composition of germanium selenide.

5. The memory cell of claim 1 wherein the conductive material of the first, second and third electrodes is the same.

6. The memory cell of claim 1 wherein the thickness of the first layer of a metal-doped chalcogenide material is less than the thickness of the second layer of a metal-doped chalcogenide material.

7. The memory cell of claim 1 wherein the thickness of the second layer of a metal-doped chalcogenide material is less than the thickness of the first layer of a metal-doped chalcogenide material.

8. The memory cell of claim 1, further comprising:

a fourth electrode formed from a fourth conductive material; and

a third layer of a metal-doped chalcogenide material disposed between the third and fourth electrode layers, the third layer providing a medium in which a conductive growth can be formed to electrically couple together the third and fourth electrodes.

9. The memory cell of claim 1 wherein the metal-doped chalcogenide material of the first and second layers are the same.

10. The memory cell of claim 1 wherein the metal-doped chalcogenide material of the first and second layers comprise a silver glass material.

11. A multiple-state memory cell, comprising:

a first electrode coupled to a first voltage;

a second electrode coupled to a second voltage;

a multiple layer data state stack in which multiple data states are stored, the data-state stack including:

a first portion of a metal-doped chalcogenide material adjoining the first electrode, the first portion having a first thickness;

a third electrode of a conductive material adjoining the first portion; and

a second portion of a metal-doped chalcogenide material adjoining the third electrode, the second portion having a second thickness,

wherein application of a programming voltage to the first electrode induces the formation of a first conductive growth from the third electrode to the first electrode and a second conductive growth from the second electrode to the third electrode.

12. The memory cell of claim 11 wherein the first voltage is positive relative to the second voltage.

13. The memory cell of claim 11 wherein the first voltage is negative relative to the second voltage.

14. The memory cell of claim 11 wherein the first portion is positioned below the third electrode, and the third electrode is positioned below the second portion.

15. The memory cell of claim 11 wherein the first portion is positioned laterally adjacent to the third electrode, and the third electrode is positioned laterally adjacent to the second portion.

16. The memory cell of claim 11 wherein the first thickness is less than the second thickness.

17. The memory cell of claim 11 wherein under the application of the programming voltage, the first conductive growth couples the third electrode to the first electrode prior to the second conductive growth coupling the second electrode to the third electrode.

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18. A multiple state memory cell, comprising:

a first electrode layer formed from a first conductive material;

a second electrode layer formed from a second conductive material;

a first layer of a metal-doped chalcogenide material disposed between and adjoining the first and second electrode layers, the first layer providing a medium in which a conductive growth can be formed to electrically couple together the first and second electrode layers;

a third electrode layer formed from a third conductive material;

a second layer of a metal-doped chalcogenide material disposed between and adjoining the second and third electrode layers, the second layer providing a medium in which a conductive growth can be formed to electrically couple together the second and third electrode layers;

a fourth electrode layer formed from a fourth conductive material; and

a third layer of a metal-doped chalcogenide material disposed between and adjoining the third and fourth electrode layers, the third layer providing a medium in which a conductive growth can be formed to electrically couple together the third and fourth electrode layers.

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19. The memory cell of claim 18 wherein at least one of the first, second, third, and fourth electrode layers comprises a composition of a silver material.

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20. The memory cell of claim 18 wherein the first, second, third, and fourth conductive material are the same.

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21. The memory cell of claim 18 wherein the thickness of the first layer of a metal-doped chalcogenide material is less than the thickness of the second layer of a metal-doped chalcogenide material, and the thickness of the second layer of a metal-doped chalcogenide material is less than the thickness of the third layer of a metal-doped chalcogenide material.

22. The memory cell of claim 18 wherein the metal-doped chalcogenide material of the first, second, and third layers are the same.

23. The memory cell of claim 18 wherein the metal-doped chalcogenide material of at least one of the first, second, or third layers comprises a material selected from the group consisting of germanium selenide, arsenic sulfide, germanium telluride, and germanium sulfide.

24. The memory cell of claim 18 wherein the metal-doped chalcogenide material of at least one of the first, second, or third layers comprises a composition of germanium selenide.

25. The memory cell of claim 18 wherein the first electrode is positioned below the second electrode, the second electrode is positioned below the third electrode, and the third electrode is positioned below the fourth electrode.

26. The memory cell of claim 18 wherein under the application of the programming voltage, the first conductive growth couples the third electrode to the first electrode prior to the second conductive growth coupling the second electrode to the third electrode.

27. A memory device, comprising:

a memory array comprising a plurality of memory cells arranged in rows and columns, each memory cell comprising:

a first electrode layer formed from a first conductive material and coupled to a respective row;

a second electrode layer formed from a second conductive material;

a first layer of a metal-doped chalcogenide material disposed between and adjoining the first and second electrode layers, the first layer providing a medium in which a

conductive growth can be formed to electrically couple together the first and second electrode layers;

a third electrode layer formed from a third conductive material and coupled to a respective column; and

a second layer of a metal-doped chalcogenide material disposed between and adjoining the second and third electrode layers, the second layer providing a medium in which a conductive growth can be formed to electrically couple together the second and third electrode layers;

a row address decoder for selecting a row of memory cells corresponding to a row address;

a column address decoder for selecting a column of memory cells corresponding to a column address;

reading and writing circuitry coupled to the memory array to read data from and write data to the memory cells selected by the row and column address decoders;

a data path coupled between the reading and writing circuitry and an external data terminal of the memory device; and

a command decoder operable to generate control signals responsive to memory commands applied to the memory device.

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28. The memory device of claim 27 wherein the first conductive layer of each memory cell is formed from a composition of a silver material.

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29. The memory device of claim 27 wherein the conductive material of the first, second and third electrodes is the same.

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30. The memory device of claim 27 wherein the thickness of the first layer of a metal-doped chalcogenide material is less than the thickness of the second layer of a metal-doped chalcogenide material.

31. The memory device of claim 27 wherein each memory cell further comprises:

a fourth electrode formed from a fourth conductive material; and

a third layer of a metal-doped chalcogenide material disposed between the third and fourth electrode layers, the third layer providing a medium in which a conductive growth can be formed to electrically couple together the third and fourth electrodes.

32. The memory device of claim 27 wherein the metal-doped chalcogenide material of the first and second layers are the same.

33. The memory device of claim 27 wherein the metal-doped chalcogenide material of the first and second layers comprise a silver glass material.

34. The memory device of claim 27 wherein the metal-doped chalcogenide material of at least one of the first or second layers comprises a material selected from the group consisting of germanium selenide, arsenic sulfide, germanium telluride, and germanium sulfide.

35. The memory cell of claim 27 wherein the metal-doped chalcogenide material of at least one of the first or second layers comprises a composition of germanium selenide.

36. A memory device, comprising:

a memory array comprising a plurality of memory cells arranged in rows and columns, the memory cells comprising:

a first electrode coupled a respective row;

a second electrode coupled to a respective column;

a multiple layer data state stack in which multiple data states are stored, the data-state stack including:

a first layer of a metal-doped chalcogenide material adjoining the first electrode, the first layer having a first thickness;

a third electrode layer of a conductive material adjoining the first layer; and

a second layer of a metal-doped chalcogenide material adjoining the third electrode layer, the second layer having a second thickness,

wherein application of a programming voltage to the first electrode induces the formation of a first conductive growth from the third electrode layer to the first electrode and a second conductive growth from the second electrode too the third electrode layer;

a row address decoder for selecting a row of memory cells corresponding to a row address;

a column address decoder for selecting a column of memory cells corresponding to a column address;

reading and writing circuitry coupled to the memory array to read data from and write data to the memory cells selected by the row and column address decoders;

a data path coupled between the reading and writing circuitry and an external data terminal of the memory device; and

a command decoder operable to generate control signals responsive to memory commands applied to the memory device.

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37. The memory device of claim 36 wherein the first voltage is positive relative to the second voltage.

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38. The memory device of claim 36 wherein the first portion is positioned below the third electrode, and the third electrode is positioned below the second portion.

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39. The memory device of claim 36 wherein the first portion is positioned laterally adjacent to the third electrode, and the third electrode is positioned laterally adjacent to the second portion.

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40. The memory device of claim 36 wherein the first thickness is less than the second thickness.

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41. The memory device of claim 36 wherein under the application of the programming voltage, the first conductive growth couples the third electrode to the first electrode prior to the second conductive growth coupling the second electrode to the third electrode.

42. A method of storing multiple data states in a memory, comprising:

to store a first data state, short circuiting a first electrode to a second electrode to change a resistance from an initial resistance to a first resistance;

to store a second data state, short circuiting the second electrode to a third electrode to change the first resistance to a second resistance; and

to store a third data state, substantially maintaining the initial resistance between the first and second electrodes and the second and third electrodes.

43. The method of claim 42 wherein short circuiting the first electrode to a second electrode comprises applying a programming voltage to induce the formation of a conductive growth from the first electrode that couples the first electrode to the second electrode and wherein short circuiting the second electrode to the third electrode comprises applying the programming voltage to induce the formation of a conductive growth from the second electrode that couples the second electrode to the third electrode.

44. The method of claim 43 wherein under the application of the programming voltage the first electrode is short circuited to the second electrode prior to the second electrode short circuiting to the third electrode.

45. The method of claim 42, further comprising to store a fourth data state, short circuiting the third electrode to a fourth electrode to change the second resistance to a third resistance.

46. A method for forming a multiple state memory cell, comprising:

forming a first electrode layer from a first conductive material;

forming a first layer from a metal-doped chalcogenide material on the first electrode layer,

forming a second electrode layer from a second conductive material on the first layer;

forming a second layer from a metal-doped chalcogenide material on the second electrode layer; and

forming a third electrode layer from a third conductive material on the second layer,

the first layer providing a medium in which a conductive growth can be formed to electrically couple together the first and second electrode layers and the second layer providing a medium in which a conductive growth can be formed to electrically couple together the second and third electrode layers.

47. The method of claim 46 wherein forming the first electrode layer comprises forming the first electrode layer from a composition of a silver material.

48. The method of claim 46 wherein forming the first and second electrode layers comprises forming the first and second electrodes from the same type of material.

49. The method of claim 46 wherein forming the first layer and forming the second layer comprises forming the first layer having a thickness less than the thickness of the second layer.

50. The method of claim 46 wherein forming the first layer and forming the second layer comprises forming the first layer having a thickness greater than the thickness of the second layer.

51. The method of claim 46, further comprising:

forming a third layer of a metal-doped chalcogenide material on the third electrode layer; and

forming a fourth electrode formed from a fourth conductive material on the third layer, the third layer providing a medium in which a conductive growth can be formed to electrically couple together the third and fourth electrode layers.

52. The method of claim 46 wherein the metal-doped chalcogenide material of the first and second layers are the same.

53. The method of claim 46 wherein the metal-doped chalcogenide material of at least one of the first or second layers comprises a material selected from the group consisting of germanium selenide, arsenic sulfide, germanium telluride, and germanium sulfide.

54. The memory cell of claim 46 wherein the metal-doped chalcogenide material of at least one of the first or second layers comprises a composition of germanium selenide.

55. The method of claim 46 wherein the first electrode is formed beneath the first layer, the first layer is formed beneath the second electrode, the second electrode is formed beneath the second layer, and the second layer is formed beneath the third electrode layer.

56. The method of claim 46 wherein the first electrode is formed adjacent the first layer, the first layer is formed adjacent the second electrode, the second electrode is formed adjacent the second layer, and the second layer is formed adjacent the third electrode layer.